



Substitute for Form 1449/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

Page 1 of 4

<b>Application No.</b>	09/837,307
<b>Filed</b>	4/17/2001
<b>First Inventor</b>	Garrett, Jr., Billy
<b>Art Unit</b>	2187-2189
<b>Examiner</b>	Dinh, Ngoc V.
<b>Atty. Docket No.</b>	RBS2.P031

U.S. Patent Documents					
Examiner Initials*	US Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines
	Number	Kind			
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	4670745		O'Malley et al.	Jun., 1987	
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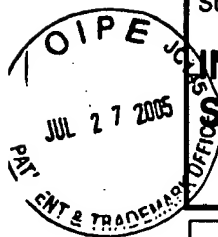
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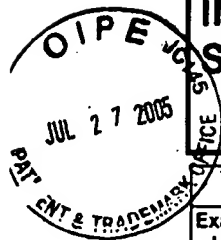
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	Number	Kind				
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ND	GB2367400	A		4/3/2002		

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**Non Patent Literature Documents**

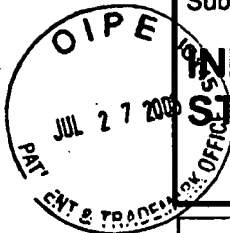
Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans- lation
ND	C. Yoo et al., "A 1.8V 700 Mb/s/pin 512Mb DDR-II SDRAM with On-Die Termination and Off-Chip Driver Calibration, IEEE International Solid-State Circuits Conference ISSCC 2003/Session 17/SRAM and DRAM/ Paper 17.7, pp. 312-313 and 496, plus Visuals Supplement on pp. 250-251 and 535	
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	<del>IEEE 100, "The Authoritative Dictionary of IEEE Standards Terms", Seventh Edition. Critical piece first to Cross bar switch (page 252).</del>	
ND	Kirihata et al., "A 390-mm <sup>2</sup> , 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture", IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999; pages 1580-1588	
ND	Masumoto, "Configurable On-Chip RAM Incorporated Into High Speed Logic Array", Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, May 20-23, 1985; pages 240-243.	
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Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans- lation
MP	S. Takase and N.i Kushiya, "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE Journal of Solid State Circuits, Vol. 34, No. 11, November 1999, pp. 1600-1606	
	<del>S. Takase and N.i Kushiya, "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE International Solid-State Circuits Conference, 4 pages plus ISSCC Slide Supplement pp. 348-349 and 506-507</del>	
	<del>Samsung Electronics, "SDRAM Device Operations," 41 pages, date unknown.</del>	
MP	Satoh et al., "A 209K-Transistor ECL Gate Array with RAM", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989; pages 1275-1281.	
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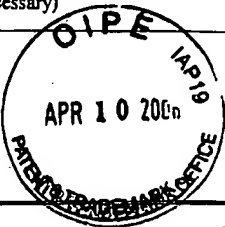
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Examiner Initials*	US Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines
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ND	EP 1248267A			10/9/2002		

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Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans- lation
ND	International Search Report and Written Opinion of the International Searching Authority in International Application PCT/US2005/028728, World Intellectual Property Organization, January 4, 2006	


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<b>Substitute for Form 1449A/PTO (Modified)</b> (use as many sheets as necessary)				<b>Attorney Docket No.:</b> RBS2.P031		<b>Application Number:</b> 09/837,307	
				<b>First Named Inventor:</b> Billy Garrett, Jr.		<b>RECEIVED</b> APR 13 2006	
				<b>Filing Date:</b> April 17, 2001		<b>Group:</b> 3487 2189 Technology Center 2100	
<b>U.S. PATENT DOCUMENTS</b>							
Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number	Kind Code <sup>2</sup> (If known)				
ND		2004/0120197	A1	Kondo et al.	06-24-2004		
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<b>FOREIGN PATENT DOCUMENTS</b>								
Exam. Initial*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (If known)				
ND		WO	91/16680	A1	Rambus, Inc.	10/31/1991		


<b>NON PATENT LITERATURE DOCUMENTS</b>			
Exam. Initial*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>7</sup>
ND		International Search Report and Written Opinion of the International Searching Authority in International Application PCT/US2005/032770, World Intellectual Property Organization, January 26, 2006, 12 pgs.	

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Substitute for Form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  Page 1 of 5	<b>Application No.</b>	09/837,307
	<b>Filed</b>	4/17/2001
	<b>First Inventor</b>	Garrett, Jr., Billy
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Examiner Initials*	US Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication	Relevant Pages, Columns, Lines
	Number	Kind			
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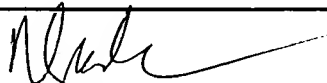
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ND	AIMOTO et al., "SP23.3: a 7168GIPS 3.84GB/s 1W Parallel Image-Processing RAM Integrating a 16Mb DRAM and 128 Processors," ISSCC, Feb. 1996, pp. 372-373/476.	
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ND	GIACALONE et al., "SP23.2: A 1MB 100MHz Integrated L2 Cache Memory with 128b Interface and ECC Protection," ISSCC, Feb. 1996, pp. 370-371/475.	
ND	HIROSE, et al., "A 20-ns 4-Mb COMOS SRAM with Hierarchical Word Decoding Architecture," IEEE, Oct. 1990, pp 1068-1072. Vol. 25, No. 5.	
ND	JEDEC, "Minutes of Meeting No. 71, JC-42.3 Committee on RAM Memories, including Proposal to Add Number of Banks Option to the Mode Register for 64M SDRAM," Joint Electron Device Engineering Council (JEDEC), 5/25/1994, New York, NY, pp. 1-14 plus 2-pg. Attachment T	
ND	KIOKE et al., "SP23.1: A 60-ns 1Mb Nonvolatile Ferroelectric Memory with Non-Driven Cell Plate Line Write/Read Scheme," ISSCC, Feb. 1996, pp. 368-379/475.	
ND	KONISHI et al., "Session SVIII: Static RAMs - FAM18.6: A 64Kb COMOS RAM," ISSCC, Feb. 1982, pp. 258-259/333.	
ND	Micron Graphics DDR3 DRAM. Advance 256Mb: x 32 GDRA3 DRAM. © 2003 Micron Technology, Inc., pages 1-67.	
ND	NAKAMURA et al., "FA14.2: A 29ns 64Mb DRAM with Hierarchical Array Architecture," ISSCC, Feb. 1995, pp. 246-247/373.	

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<b>Examiner Signature</b>		<b>Date Considered</b>	12/03/07
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.